Remarks

The Final Office Action dated April 1, 2010, notes the following new grounds of rejection: claims 1 and 7 stand rejected under 35 U.S.C. § 112(2); claims 1, 5-8 and 10-14 stand rejected under 35 U.S.C. § 103(a) over Thuringer (U.S. Patent No. 6,498,404) in view of Odinak (U.S. Patent No. 6,419,159) and further in view of AAPA; and claims 2-4 stand rejected under 35 U.S.C. § 103(a) over the '404 and '159 references and AAPA, and further in view of the Patterson reference ("Computer Architecture: A Quantitative Approach", pp. 134-135, 1995). In this discussion set forth below, Applicant does not acquiesce to any rejection or averment in this Office Action unless Applicant expressly indicates otherwise.

Applicant respectfully traverses the unsupported § 112(2) rejections of claims 1 and 7. The Office Action asserts that "each of the pairs of processing signals including an input signal and an output signal of one of the processing circuits" is unclear and ambiguous. However, one of ordinary skill in the art would find the plain meaning of this limitation is clear. Further, the asserted reason for this ambiguity is based on Applicant's arguments, which is not a proper basis for a § 112(2) rejection. *See* M.P.E.P. §§ 706.03(d) and 2173. Notwithstanding the above, nothing in Applicant's previous arguments appears to Applicant to make the cited portion of the claims unclear, and the rejection has not pointed out with any specificity which arguments the Office Action relies on in presenting the new § 112(2) rejection. Accordingly, the §112(2) rejection is improper and should be removed.

Applicant respectfully traverses the § 103(a) rejections of all claims for lack of correspondence. For example, certain aspects of the claimed invention are directed to an activity monitor circuit which receives pairs of processing signals, "each of the pairs of processing signals including an input signal and an output signal of one of the processing circuits." The Office Action relies on paragraph five of Applicant's published application to teach a pair of processing signals including an input signal and an output signal of one of the processing circuits. However, the AAPA cited does not teach a pair of processing signals, but rather a feedback loop. One of skill in the art would understand a feedback loop to use the output of the processor signal as one of the inputs of the

processor signal. Accordingly, the asserted combination fails to correspond to certain aspects of the claimed invention and the § 103(a) rejections must be withdrawn.

The asserted hypothetical combination of references further lacks correspondence to activity information derived from the pair of processing signals that indicates whether the processing circuit generates a logic level transition. The Office Action cites the AAPA as teaching monitoring the logic level changes of the circuit. However, the asserted portions of Applicant's specification do not disclose monitoring of logic level transitions. Instead, paragraphs 3 and 4, which discuss logic levels are discussing WO 00/26746, which is the parent application to the asserted '404 reference. The AND gates of the '404 reference do not determine a logic level transition of one of the AND gates, instead the '404 reference teaches that the output of "AND-gate 8 switches to '1' when the inputs of the first AND gate are all of logic value '0'." There is no mention of a change in output of the first AND gate, nor of the second AND gate (asserted as the monitor in the Office Action) determining a transition in the logic level (output) of AND gate 5. Accordingly, the asserted hypothetical embodiment lacks correspondence. Therefore, the § 103(a) rejection is improper and should be removed.

Moreover, as Applicant has previously pointed out, the proposed combination of the '404 and '159 references does not correspond to the claimed invention. The addition of the AAPA, which is primarily duplicative of the '404 reference, does nothing to fix this lack of correspondence. Applicant respectfully submits that the rejections appear to be based primarily on the Office Action's misunderstanding of the operation of the cited embodiment of the '404 reference. In particular, the cited embodiment of the '404 reference does not teach separate current drawing and activity monitor circuits, with the current drawing circuit being controlled by the activity monitor circuit based on a combined activity signal derived by the activity monitor circuit as claimed. The Office Action continues to rely upon the load circuit discussed in Col. 1:28-38 of the '404 reference as allegedly corresponding to Applicant's current drawing circuit while failing to recognize that this load circuit is in fact the complementary gates (*e.g.,* AND gate 8 of Fig. 2) that are alleged to correspond to Applicant's activity monitor circuit. *See, e.g.,* Col. 1:45-52 and Col. 2:39-57. As such, the cited load circuit of the '404 reference does not correspond to Applicant's current drawing circuit. Applicant also notes that the

complementary gates of the '404 reference function independently from one another and, as such, Applicant fails to see how the Examiner argues that these complementary gates do necessarily derive a combined activity signal indicative of a sum of power supply currents consumed by multiple processing circuits as in Applicant's claimed activity monitor circuit. Accordingly, the § 103(a) rejections of claims 1-8 and 10-14 are improper and should be withdrawn.

Applicant further traverses the § 103(a) rejections of claims 1-8 and 10-14 because the Examiner fails to provide a valid reason for the proposed combination of the '404 and '159 references, thus also failing to cite evidence of motivation for modifying the '404 reference. Consistent with M.P.E.P. § 2143.01 and relevant case law, a § 103 rejection must provide evidence of motivation where a proposed combination of references would modify a primary reference. *See, e.g., See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (U.S. 2007). ("A patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art."). In this instance, the Examiner asserts that the skilled artisan would modify the '404 reference to include the random current drawing circuitry 40 of the '159 reference to "increase the security of the system by making the output power supply based on the randomness of the current sinks instead of making the output power supply constant as in (the '404 reference)." *See* page 7 of the instant Office Action. However, this hypothetical combination lacks any supporting evidence, and further does not provide a clearly-articulated reason that would be consistent with the *KSR* decision. In particular, the '404 reference teaches that it is the constant power consumption that disguises the actual power consumed by the data carrier during security-relevant operations. *See, e.g.,* Col. 1:45-65. The Office Action fails to present any evidence that the modification of the '404 reference would "increase the security of the system" relative to the unmodified '404 reference which already disguises the actual power consumed by the data carrier during security-relevant operations using complementary logic. As such, the Office Action's proposed modification involves adding redundant circuitry to the '404 reference without any perceived benefit.

In responding to Applicant's previous arguments regarding the combination of the '404 reference and the '159 reference, the Office Action asserts that the two references

teach different ways to mask the power supply fluctuations, and therefore it would be obvious to replace one with the other. This assertion ignores the technical difficulties of modifying the '404 reference. More specifically, the proposed combination involves extensively modifying the '404 reference to somehow implement the random current drawing circuitry 40 of the '159 reference. Accordingly, the Examiner's assertion of such a vague "articulated reasoning" (*e.g.*, to "increase the security of the system") in support of the modification is insufficient, particularly in view of the fact that the Office Action fails to present any evidence that the proposed combination would "increase the security of the system" relative to the unmodified '404 reference. *KSR* and M.P.E.P. § 2141 make it clear that such assertions are inapplicable where the operation of one of the references is modified. *See, e.g., KSR* 550 U.S. at 417. For example, according to M.P.E.P. § 2141, Applicant can rebut such assertions of obviousness simply by showing that "the elements in combination do not merely perform the function that each element performs separately." This is also consistent with various parts of *KSR*, which repeatedly refer to combined teachings in which the cited references are not modified in their operation. Accordingly, the § 103(a) rejections of claims 1-8 and 10-14 are improper and Applicant requests that they be withdrawn.

Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Juergen Krause-Polstorff, of NXP Corporation at (408) 474-9062.

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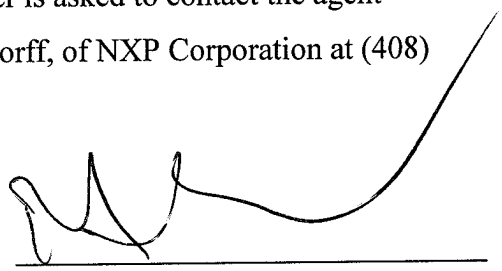
By: 

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